KIT - Kalaignarkarunanidhi Institute of Technology

An Autonomous Institution

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

Accredited by NAAC with 'A' GRADE & NBA (AERO, CSE, ECE, EEE, MECH & MBA)

An ISO 9001 : 2015 Certified Institution, Coimbatore - 641 402.

Regulations, Curriculum & Syllabus - 2023

(For Students admitted from the Academic Year 2023-24 and onwards)

MASTER OF ENGINEERING DEGREE

IN

VLSI DESIGN

Department of Electronics and Communication Engineering

PG – VLSI Design

	Conceptual Framework (For Students admitted from theAcademicYear2023-24onwards)	

Semester	Level of Course	Hours /Week	No of Courses	Range of Credits/ Courses	Total Credits
PART I					
A – Foundation Courses					
I	Foundation Courses **(FC)**	4	1	4	4
B – Professional Core Courses					
I to III	Professional Core**(PC)**	3	11	2-3	31
C – Elective Courses					
II to III	Professional Elective**(PE)**	3	5	3	15
D – Project Work					
III & IV	Project Work**(PW)**	12-24	2	6-12	18
PART II- Career Enhancement Courses(CEC)					
II	Article Writing and Seminar	2	1	1	1
Total Credit					**69**

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Curriculum and Scheme of Assessment

(For Students admitted from the Academic Year 2023-24 and onwards)

Semester I

Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
Theory / Theory with Practical										
M23MAT105	Graph Theory and Optimization Techniques	FC	4	3	1	0	4	40	60	100
M23VDT101	CMOS Digital VLSI Design	PC	3	3	0	0	3	40	60	100
M23VDT102	FPGA Based System Design	PC	3	3	0	0	3	40	60	100
M23VDT103	CAD for VLSI Circuits	PC	3	3	0	0	3	40	60	100
M23VDT104	Analog IC Design	PC	3	3	0	0	3	40	60	100
M23CST101	Research methodology and IPR	PC	3	3	0	0	3	40	60	100
Practical										
M23VDP101	VLSI Design Laboratory - I	PC	4	0	0	4	2	60	40	100
Total credits to be earned							**21**			

Semester II

Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
Theory / Theory with Practical										
M23VDT201	Device Modeling	PC	3	3	0	0	3	40	60	100
M23VDT202	DSP Structures for VLSI	PC	3	3	0	0	3	40	60	100
M23VDT203	Low Power VLSI Design	PC	3	3	0	0	3	40	60	100
	Professional Elective-I	PE	3	3	0	0	3	40	60	100
	Professional Elective-II	PE	3	3	0	0	3	40	60	100
	Professional Elective -III	PE	3	3	0	0	3	40	60	100
Practical										
M23VDP201	VLSI Design Laboratory - II	PC	4	0	0	4	2	60	40	100
M23CEP203	Article Writing and Seminar	CEC	2	0	0	2	1	100	-	100
Total credits to be earned							**21**			

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Semester III										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
Theory / Theory with Practical										
M23VDT301	Testing of VLSI Circuits	PC	3	3	0	3	3	40	60	100
	Professional Elective -IV	PE	3	3	0	3	3	40	60	100
	Professional Elective-V	PE	3	3	0	3	3	40	60	100
Practical										
M23VDP301	Project Work (Phase I)	PW	12		0	12	6	40	60	100
Total credits to be earned							**15**			

Semester IV										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
Practical										
M23VDP401	Project Work (Phase II)	PW	24	0	0	24	12	40	60	100
Total credits to be earned							**12**			

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FOUNDATIONCOURSES(FC)										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23MAT105	Graph Theory and Optimization Techniques	FC	4	3	1	0	4	40	60	100

PROFESSIONALCORE(PC)										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDT101	CMOS Digital VLSI Design	PC	3	3	0	0	3	40	60	100
M23VDT102	FPGA Based System Design	PC	3	3	0	0	3	40	60	100
M23VDT103	CAD for VLSI Circuits	PC	3	3	0	0	3	40	60	100
M23VDT104	Analog IC Design	PC	3	3	0	0	3	40	60	100
M23CST101	Research Methodology and IPR	PC	3	3	0	0	3	40	60	100
M23VDP101	VLSI Design Laboratory - I	PC	4	0	0	4	2	60	40	100
M23VDT201	Device Modeling	PC	3	3	0	0	3	40	60	100
M23VDT202	DSP Structures for VLSI	PC	3	3	0	0	3	40	60	100
M23VDT203	Low Power VLSI Design	PC	3	3	0	0	3	40	60	100
M23VDP201	VLSI Design Laboratory - II	PC	4	0	0	4	2	60	40	100
M23VDT301	Testing of VLSI Circuits	PC	3	3	0	0	3	40	60	100

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PROFESSIONALELECTIVE (PE)										
SEMESTER – II										
ELECTIVE – I										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDE201	VLSI Technology	PE	3	3	0	0	3	40	60	100
M23AEE101	Computer Architecture and Parallel Processing	PE	3	3	0	0	3	40	60	100
M23AET301	Advanced Microprocessors and Microcontrollers Architecture	PE	3	3	0	0	3	40	60	100
M23AEE103	Neural Networks and Applications	PE	3	3	0	0	3	40	60	100
SEMESTER – II										
ELECTIVE – II										
M23VDE202	DSP Integrated Circuits	PE	3	3	0	0	3	40	60	100
M23VDE203	Nano Electronics	PE	3	3	0	0	3	40	60	100
M23AEE201	High Performance Networks	PE	3	3	0	0	3	40	60	100
M23AEE202	Wireless Adhoc and Sensor Networks	PE	3	3	0	0	3	40	60	100

SEMESTER – II										
ELECTIVE – III										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDE204	System on Chip Design	PE	3	3	0	0	3	40	60	100
M23AET201	Soft Computing and Optimization Techniques	PE	3	3	0	0	3	40	60	100
M23VDE205	Reconfigurable Architectures	PE	3	3	0	0	3	40	60	100
M23VDE206	Signal Integrity for High Speed Networks	PE	3	3	0	0	3	40	60	100

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SEMESTER – III										
ELECTIVE – IV										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDE301	Principles of Remote Sensing	PE	3	3	0	0	3	40	60	100
M23AEE303	Advanced Digital Image Processing	PE	3	3	0	0	3	40	60	100
M23AEE304	Pattern Recognition	PE	3	3	0	0	3	40	60	100
M23AET202	Embedded System Design	PE	3	3	0	0	3	40	60	100

SEMESTER – III										
ELECTIVE – V										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDE305	MEMS and NEMS	PE	3	3	0	0	3	40	60	100
M23AET203	Hardware-Software Co-Design	PE	3	3	0	0	3	40	60	100
M23AEE205	Robotics	PE	3	3	0	0	3	40	60	100
M23VDE306	Machine Learning and Algorithm design	PE	3	3	0	0	3	40	60	100
PROJECT WORK (PW)										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDP301	Project Work(Phase I)	PW	12	0	0	12	6	40	60	100
M23VDP401	Project Work(Phase II)	PW	24	0	0	24	12	40	60	100

CAREER ENHANCEMENT COURSE(CEC)										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23CEP203	Article Writing and Seminar	CEC	2	0	0	2	1	100	-	100

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M.E. VLSI	M23MAT105 GRAPH THEORY AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	1	0	4

Course Objectives	
1.	To understand and apply the fundamental concepts in graph theory.
2.	To determine spanning tree, employ the algorithms to find minimum spanning tree, shortest path of a graph and maximum flow.
3.	To formulate and solve LPP.
4.	To solve transportation and assignment problems.
5.	To introduce network modeling for planning and scheduling the project activities.

UNIT – I GRAPH THEORY	12
Common families of graphs, degree sequence, handshaking lemma, Havel-Hakimi theorem (statement only).Walk, trail and path, connected graph, distance, radius and diameter. Graph isomorphism. Representations of graphs - adjacency and incidence lists - adjacency and incidence matrices.	

UNIT – II GRAPH ALGORITHMS	12
Trees, spanning trees. Search algorithms - depth first search and breadth first search, spanning tree algorithm - Kruskal's and Prim's, shortest path algorithm - Dijkstra's flow networks: flows and cuts in networks, solution of the maximum - flow problem - characterization of maximum flow - Max-flow Min-cut Theorem (statement only), algorithms - maximum flow, augmenting path, and FFEK - maximum flow.	

UNIT – III LINEAR PROGRAMMING	12
Mathematical Formulation of LPP - Graphical solution to Linear Programming Problems - Simplex method – Big M method - Two phase method – Principles of Duality - Dual Simplex Method.	

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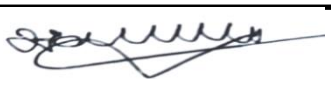
UNIT – IV TRANSPORTATION AND ASSIGNMENT PROBLEM	12
Mathematical formulation of transportation problem - Methods for finding initial basic feasible solution - optimum solution - degeneracy - Mathematical formulation of assignment models - Hungarian Algorithm.	

UNIT – V NETWORK ANALYSIS	12
Network Construction - Critical Path Method - Project Evaluation and Review Technique - Resource Analysis in Network Scheduling.	
	Total Instructional hours : 60

Course Outcomes : Students will be able to	
CO1	Make use of principles and concepts of graph theory in practical situations……..
CO2	Apply minimum cost spanning tree algorithm on the graph and apply single source shortest path to find the shortest path from source vertex.
CO3	Constructs linear programming model.
CO4	Solve transportation and assignment problems to get the optimal solutions.
CO5	Construct the network modeling for planning and scheduling the project activities.

Reference Books	
1.	Douglas B West, “Introduction to graph Theory”, Pearson Education, New Delhi, 2018.
2.	Narasingh Deo, “Graph Theory: with applications to engineering and computer science”, PHI Learning, 2017.
3.	Taha, H.A., “Operations Research: An Introduction”, Pearson education, Asia, New Delhi, 9th Edition, 2016.
4.	Kambo N.Singh., “Mathematical Programming Techniques”, East – West Press, New Delhi, 2012.
5.	N. D Vohra, Quantitative Techniques in Management, TataMcgraw Hill, 5 th Edition, 2017.



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M.E.	M23VDT101-CMOS DIGITAL VLSI DESIGN (Common to VLSI & AE)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To introduce the principle of operation of CMOS inverter.
2.	To study the concept of combinational logic circuits.
3.	To study the concept of sequential logic circuits.
4.	To introduce the architectures of VLSI system.
5.	To learn about the interconnect and clocking process.

UNIT-I	MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER	9

MOS(FET)Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy and Energy Delay parameters.

UNIT-II	COMBINATIONAL LOGIC CIRCUITS	9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT-III	FIELD EFFECT TRANSISTORS	9

Drain and Transfer characteristics, Current equations, Pinch off voltage and significance of JFET, Drain and Transfer Characteristics, Threshold voltage, Channel length modulation of MOSFET, Comparison of MOSFET with JFET.

UNIT-IV	SPECIAL SEMICONDUCTOR DEVICES	9

MESFET, FINFET, PINFET, CNTFET, Schottky barrier diode, Zener diode, Varactor diode, Tunnel diode, LASER diode and LDR.

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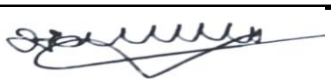
UNIT-V	POWER DEVICES AND DISPLAY DEVICES	9
UJT, SCR, Diac, Triac, Power BJT, LED, LCD, Phototransistor, Opto Coupler, Solar cell.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Explain the V-I characteristic of PN diode
CO2	Describe the models and equivalence circuits of Bipolar Junction Transistors
CO3	Explain the characteristic of Field Effect Transistors
CO4	Operate the Special Semiconductor Devices such as MESFET, FINFET, LASER diode and LDR
CO5	Operate the basic electronic devices such as power Bipolar Transistors, Power control devices, LED, LCD and other Optoelectronic devices

Text Books	
1.	Jan Rabaey, Anantha Chandrakasan, B Nikolic, “Digital Integrated Circuits: A Design Perspective”. Second Edition, Feb 2003, Prentice Hall of India.
2.	Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, Wiley IEEE Press 2010 3rd Edition.

Reference Books	
1.	M J Smith, “Application Specific Integrated Circuits”, Addisson Wesley, 1997.
2.	N.Weste, K. Eshraghian, “Principles of CMOS VLSI Design”. Second Edition, 1993 Addision Wesley.



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M.E	M23VDT102 - FPGA BASED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To understand the automated design flow for designs with FPGAs
2.	To understand the Digital system design using HDL.
3.	To understand the FPGA architecture, interconnect and technologies.
4.	To analyze the area and power of the architectures
5.	To understand configuring and implementing digital embedded system on FPGA.

UNIT-I	FPGA DESIGN FLOW AND ARCHITECTURES	9

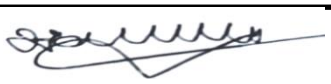
Digital IC design flow-The role of FPGAs in digital design–Goals and techniques–Hierarchical design-CAD Tools. FPGA architectures–Configurable logic blocks-configurable I/O blocks– Programmable interconnect–clock circuitry–Xilinx FPGA architecture–Programming Technologies: Antifuse, SRAM, EPROM, EEPROM.

UNIT-II	VERILOG HDL	9

HDL overview-Modules and ports-compiler directives-data types-operands and operators-gate level modeling-data flow modeling-behavioral modeling-structural modeling–primitives-Tasks and functions-Writing test bench.

UNIT-III	ARCHITECTING SPEED AND TIMING ISSUES	9

High Throughput - Low Latency - Timing - Add Register Layers, Parallel Structures, Flatten Logic Structures, Register Balancing, reorder Paths. CLOCKING AND METASTABILITY: Set up time hold time–setup time hold time violations-critical path-calculation of maximum clock frequency– meta stability – synchronizers design examples.



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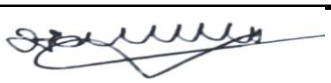
UNIT-IV	ARCHITECTING AREA AND POWER	9
Architecting Area - Rolling Up the Pipeline - Control-Based Logic Reuse - Resource Sharing - Impact of Reset on Area - Resources Without Reset, Resources Without Set, Resources Without Asynchronous Reset, Resetting RAM, Utilizing Set/Reset Flip-Flop Pins. Architecting Power - Clock Control, Clock Skew, Managing Skew, Input Control, Reducing the Voltage Supply, Dual-Edge Triggered Flip- Flops, Modifying Terminations.		

UNIT-V	EMBEDDED SYSTEM DESIGN WITH FPGA	9
Processors - Interfaces - Zynq System-on-chip Development - IP based Design - Hardware-Software Co-design for Zynq - Software Development Tools - Real-time Applications.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Understand the design mode, method, criterion and steps of FPGA design
CO2	Design and model different digital circuits with HDL
CO3	Learning the performance specification of FPGA architecture
CO4	Analyze the architecture of FPGA
CO5	Understanding about the concept of Embedded system with FPGA

Text Books	
1.	Michael D. Ciletti , "Advanced Digital Design with the Verilog HDL", Second Edition, Pearson, 2011.
2.	Steve Kilts , "Advanced FPGA Design Architecture, Implementation, and Optimization", First Edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2007.

Reference Books	
1.	Crockett H. Louise, Ross A. Elliot, Martin A. Enderwitz , "The Zynq Book Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC", First Edition, Strathclyde Academic Media, 2014.
2.	Charlet H. Roth, Lizy Kurian John, ByeongKil Lee , "Digital Systems Design using Verilog", Cengage Learning, 2016.
3.	Zainalabedin Navabi , "Verilog Digital System Design", Second Edition, McGraw-Hill Education, 2005.
4.	Ming-Bo Lin , "Digital System Designs and Practices: Using Verilog HDL and FPGAs", First Edition, Wiley, 2008.



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M.E.	M23VDT103- CAD FOR VLSI CIRCUITS (Common to VLSI & AE)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To introduce the VLSI Design methodologies.
2.	To study the algorithms related to placement and partitioning.
3.	To study the various routing and floor planning algorithms.
4.	To learn the synthesis processes understand VLSI design automation tools.
5.	To study the high level synthesis.

UNIT-I	INTRODUCTION TO VLSI DESIGN FLOW	9

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT-II	LAYOUT, PLACEMENT AND PARTITIONING	9

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning.

UNIT-III	FLOOR PLANNING AND ROUTING	9

Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT-IV	SIMULATION AND LOGIC SYNTHESIS	9

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

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UNIT-V	HIGH LEVEL SYNTHESIS	9
Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Outline the flow of VLSI design
CO2	Explain the algorithms related to placement and partitioning and layout rules
CO3	Outline floor planning and routing
CO4	Explain Simulation and Logic Synthesis
CO5	Examine the hardware models for high level synthesis

Text Books	
1.	N.A. Sherwani, “Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2.	S.H. Gerez, “Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.

Reference Books	
1.	Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World Scientific, 1999.
2.	Steven M.Rubin,“ Computer Aids for VLSI Design”, Addison Wesley Publishing,1987.

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M.E.	M23VDT104 - ANALOG IC DESIGN	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To study MOS devices modeling and scaling effects.
2.	To familiarize the design of single stage and multistage MOS amplifier.
3.	To learn and analysis frequency responses of MOS amplifiers.
4.	To introduce the concept of current mirror.
5.	To study the OPAMP circuits.

UNIT-I	MOSFET METRICS	9

Simple long channel MOSFET theory — SPICE Models — Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analogmetrics,Smallsignalparameters,UnityGainFrequency,Miller"sapproximation.

UNIT-II	SINGLE STAGE AND TWO STAGE AMPLIFIERS	9

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers — differential and common mode response, Input swing, gain, diode load and constant current load - Basic Two Stage Amplifier, Cut-off frequency, poles and zeros.

UNIT-III	FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS	9

Frequency Response of Single Stage Amplifiers — Noise in Single stage Amplifiers —Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers,–Noise in two stage Amplifiers– Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks.

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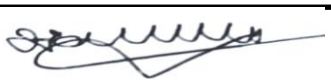
UNIT-IV	CURRENT MIRRORS AND REFERENCE CIRCUITS	9
Cascode, Negative feedback, Wilson, Regulated cascode, Band gap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design.		

UNIT-V	OPAMPS	9
Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits-Low voltage OPAMP.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Explain the basics of MOSFET circuits
CO2	Analyze the input and output impedances of stage amplifiers
CO3	Examine the Stability, frequency response and Noise in MOS amplifiers
CO4	Design the current mirror and reference circuits
CO5	Explain the characteristics of OPAMP

Text Books	
1.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2000.
2.	Philip E. Allen, “CMOS Analog Circuit Design”, Oxford University Press, 2013.

Reference Books	
1.	Paul R.Gray, “Analysis and Design of Analog Integrated Circuits”, Wiley Student edition, 5th edition, 2009.
2.	R.Jacob Baker, “CMOS: Circuit Design, Layout, and Simulation”, Wiley Student Edition, 2009.



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M.E.	M23CST101 - RESEARCH METHODOLOGY AND IPR (Common to VLSI & AE)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To impart knowledge on formulation of research problem, research methodology, ethics involved in doing research and importance of IPR protection.

UNIT-I	RESEARCH DESIGN	9

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys

UNIT-II	DATA COLLECTION AND SOURCES	9

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT-III	DATA ANALYSIS AND REPORTING	9

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

UNIT-IV	INTELLECTUAL PROPERTY RIGHTS	9

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

Approved By BoS Chairman

UNIT-V	PATENTS	9
Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
CO2	Understand research problem formulation & Analyze research related information and Follow research ethics.
CO3	Correlate the results of any research article with other published results. Write a review article in the field of engineering.
CO4	Appreciate the importance of IPR and protect their intellectual property. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Text Books	
1.	Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2.	Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.

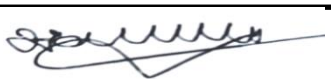
Reference Books	
1.	David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
2.	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

Approved By BoS Chairman

M.E	M23VDP101-VLSI DESIGN LABORATORY - I	L	T	P	C
		0	0	4	2

Course Objectives	
1.	The laboratory based study for the entire program is clubbed under three categories. One is the FPGA based design methodology; the second is the simulation of analog building blocks, and analog and digital CAD design flow. Experiments pertaining to the former two topics are covered in this lab course and those pertaining to the latter will be covered in VLSI Design Lab II.
2	FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms. In addition, exercises on the SPICE simulation of the basic CMOS analog building blocks will be carried out.

List of Experiments	
Expt.No.	**Description of the Experiments(Any 8 experiments)**
1.	Understanding Synthesis principles. Back annotation
2.	Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
3.	FPGA realtime programming and I/O interfacing
4.	Interfacing with Memory modules in FPGA Boards.
5.	Verification of design functionality implemented in FPGA by capturing the signal in DSO.
6.	Real time application development
7.	Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages sequential, concurrent statements and structural description
8.	Implementation of Traffic Light Controller using Verilog HDL
9.	Implementation of UVM protocol using Verilog HDL
	Total Instructional hours:60



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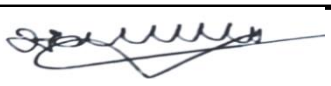
Course Outcomes: Students will be able to	
CO1	Apply FPGA Concepts in realtime applications
CO2	Examine the input output interfacing of FPGA
CO3	Design a FPGA based model for signal processing
C04	Develop a FPGA based real time model
C05	Outline about HDL

LIST OF EQUIPMENT FOR A BATCH OF 30 STUDENTS

Sl.No.	Description of the Equipment	Quantity Required (Nos.)
1.	Xilinx/ Equivalent EDA tool	15
2.	FPGA-Altera /Sparton boards	14
3.	Logic Analyzer	4
4.	DSO	4
5.	Interface Board-ADC	1
6.	DAC	1
7.	Motor Control	2
8.	SPICE Software	15



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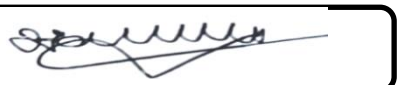
Semester II										
Course Code	Course Name	CT	InstructionalHours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
Theory / Theory with Practical										
M23VDT201	Device Modeling	PC	3	3	0	0	3	40	60	100
M23VDT202	DSP Structures for VLSI	PC	3	3	0	0	3	40	60	100
M23VDT203	Low Power VLSI Design	PC	3	3	0	0	3	40	60	100
	Professional Elective-I	PE	3	3	0	0	3	40	60	100
	Professional Elective-II	PE	3	3	0	0	3	40	60	100
	Professional Elective -III	PE	3	3	0	0	3	40	60	100
Practical										
M23VDP201	VLSI Design Laboratory - II	PC	4	0	0	4	2	60	40	100
M23CEP203	Article Writing and Seminar	CEC	2	0	0	2	1	100	-	100
Total credits to be earned							**21**			

PROFESSIONALELECTIVE (PE)										
SEMESTER – II										
ELECTIVE – I										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDE201	VLSI Technology	PE	3	3	0	0	3	40	60	100
M23AEE101	Computer Architecture and Parallel Processing	PE	3	3	0	0	3	40	60	100
M23AET301	Advanced Microprocessors and Microcontrollers Architecture	PE	3	3	0	0	3	40	60	100
M23AEE103	Neural Networks and Applications	PE	3	3	0	0	3	40	60	100
SEMESTER – II										
ELECTIVE – II										
M23VDE202	DSP Integrated Circuits	PE	3	3	0	0	3	40	60	100
M23VDE203	Nano Electronics	PE	3	3	0	0	3	40	60	100
M23AEE201	High Performance Networks	PE	3	3	0	0	3	40	60	100
M23AEE202	Wireless Adhoc and Sensor Networks	PE	3	3	0	0	3	40	60	100



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SEMESTER – II										
ELECTIVE – III										
Course Code	Course Name	CT	Instructional Hours					Assessment		
			CP	L	T	P	C	CIA	ESE	Total
M23VDE204	System on Chip Design	PE	3	3	0	0	3	40	60	100
M23AET201	Soft Computing and Optimization Techniques	PE	3	3	0	0	3	40	60	100
M23VDE205	Reconfigurable Architectures	PE	3	3	0	0	3	40	60	100
M23VDE206	Signal Integrity for High Speed Networks	PE	3	3	0	0	3	40	60	100

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M.E.	M23VDT201-DEVICE MODELLING (Common to VLSI & AE)	L	T	P	C
		3	0	0	3

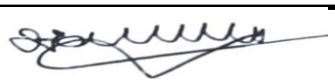
Course Objectives	
1.	To study the MOS capacitors and to model MOS Transistors.
2.	To learn about the MOSFET characteristics.
3.	To understand the various CMOS design parameters and their impact on performance of the device.
4.	To study the device level characteristics of BJT transistors.

UNIT-I	MOS CAPACITORS	9

Surface Potential: Accumulation,Depletion,andInversion,ElectrostaticPotentialandCharge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non-equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT-II	MOSFET DEVICES	9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Sub threshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields.



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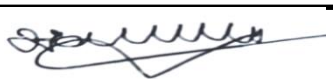
UNIT-III	CMOS DEVICE DESIGN	9
MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Non- scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Non-uniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements		

UNIT-IV	CMOS PERFORMANCE FACTORS	9
Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS		

UNIT-V	BIPOLAR DEVICES	9
N–P–N Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base– Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non- ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between BVCEO and BVCBO.		
		Total Instructional hours:45



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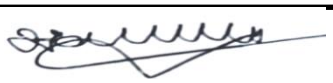
Course Outcomes: Students will be able to	
CO1	Outline the concept of MOS capacitors
CO2	Explain the operation of MOSFET with its characteristics
CO3	Design and model BJT device to desired specifications
CO4	Analyze the performance metrics of CMOS
CO5	Design and model BJT device to desired specifications

Text Books	
1.	BehzadRazavi, “Fundamentals of Micro electronics ”,Wiley Student Edition, 2nd Edition.
2.	JPCollinge,C.A.Collinge,“ Physics of Semiconductor devices”, Springer 2002 Edition.

Reference Books	
1.	Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition.



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M.E.	M23VDT202 - DSP STRUCTURES FOR VLSI	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To learn typical DSP algorithms.
2.	To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
3.	To introduce efficient design of DSP architectures suitable for VLSI.
4.	To study about numerical strength reduction.
5.	To learn typical DSP algorithms.

UNIT-I	PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS	9

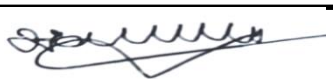
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT-II	ALGORITHMIC STRENGTH REDUCTION TECHNIQUE	9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT-III	ALGORITHIMIC STRENGTH REDUCTION -II	9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.



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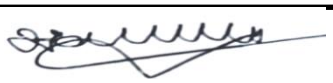
UNIT-IV	BIT-LEVEL ARITHMETIC ARCHITECTURES	9
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule,bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.		

UNIT-V	NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING	9
Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Outline the pipelining and parallel processing of DSP filters architectures
CO2	Explain the first level strength reduction techniques
CO3	Explain the first level strength reduction techniques
CO4	Analyze the various bit level arithmetic architectures
CO5	Explain the numerical strength reduction and pipelining process of filters

Text Books	
1.	Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Inter science, 2007.
2.	U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.



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M.E.	M23VDT203-LOW POWER VLSI DESIGN	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To identify sources of power in an IC.
2.	To identify the power reduction techniques based on technology independent and technology dependent.
3.	To study the low power CMOS circuits.
4.	To learn suitable techniques for power estimation.
5.	To design circuits with low power dissipation.

UNIT-I	POWER DISSIPATION IN CMOS	9

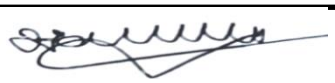
Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power –Sources of power consumption – Static Power Dissipation, Active Power Dissipation -Designing for Low Power, Circuit Techniques for Leakage Power Reduction – Basic principle of low power design

UNIT-II	POWER OPTIMIZATION	9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures- Bi CMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison.

UNIT-III	DESIGN OF LOW POWER CMOS CIRCUITS	9

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.



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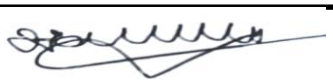
UNIT-IV	POWER ESTIMATION	9
Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.		

UNIT-V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER	9
Synthesis for low power – Behavioral level transform – software design for low power.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Explain the basics and advanced techniques in low power design
CO2	Explain the concept of power optimization
CO3	Model the low power circuits
CO4	Analyse the power estimation techniques
CO5	Design the software models for low power

Text Books	
1.	AbdelatifBelaouar, Mohamed.I.Elmasry,“Low power digital VLSI design”,Kluwer,1995.
2.	A.P.Chandrasekaran and R.W.Broadersen,“Low power digital CMOS design”,Kluwer,1995.

Reference Books	
1.	DimitriosSoudris,C.Pignet,CostasGoutis,“Designing CMOS Circuits for LowPower”,Kluwer,2002.
2.	GaryYeap,“Practical low power digital VLSI design”, Kluwer, 1998.



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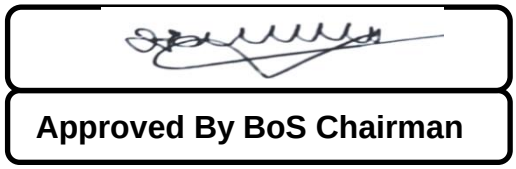
PROFESSIONAL ELECTIVE - I



Approved By BoS Chairman

M.E.	M23VDE201–VLSI TECHNOLOGY	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To understand physical and chemical processes of IC fabrication technology.
2.	To learn the various lithography techniques and concepts of wafer exposure system.
3.	To understand Concepts of thermal oxidation and different solutions to diffusion equation.
4.	To Design and evaluation of diffused layers and ion implantation.
5.	To study the importance of calibration techniques for achieving precision during dataconversion.

UNIT-I	CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION	9

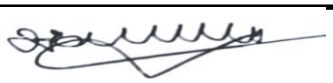
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration,Vapor Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism And kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopant At interface, Oxidation of Poly Silicon, Oxidation inducted Defects..

UNIT-II	LITHOGRAPHY AND RELATIVE PLASMA ETCHING	9

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments.

UNIT-III	DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALLIZATION	9

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one Dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques – Range Theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapors Deposition – Patterning.



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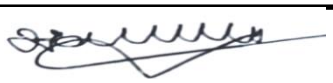
UNIT-IV	PROCESS SIMULATION AND VLSI PROCESS INTEGRATION	9
Natural response-Forced response-Transient response of RC,RL and RLC circuits to excitation by Step Signal, Impulse Signal and exponential sources, Complete response of RC, RL and RLC Circuits to sinusoidal excitation.		

UNIT-V	ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES	9
Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Understand the crystal growth and wafer fabrication.
CO2	Explain techniques used in lithography and plasma etching.
CO3	Design diffused layers and measurement methods.
CO4	Explain the simulation process and VLSI process integration.
CO5	Explain the techniques for assembly and packaging of ICs.

Text Books	
1.	S.M.Sze, “VLSI Technology”, McGraw Hill, 2nd Edition. 2008.

Reference Books	
1.	James D Plummer, Michael D. Deal, Peter B.Griffin, “Silicon VLSI Technology: fundamentals practice and Modeling”, Prentice Hall India, 2009.
2.	Wai Kai Chen, “VLSI Technology” CRC press, 2003.



Approved By BoS Chairman

M.E.	M23AEE101-COMPUTERARCHITECTURE AND PARALLEL PROCESSING (Common to AE&VLSI)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To study various types of processor architectures and the importance of scalable architectures.
2.	To introduce parallel processing and pipelining.
3.	To learn about the memory hierarchy
4.	To study the multiprocessor architecture
5.	To study the multicore architecture

UNIT-I	COMPUTER DESIGN AND PERFORMANCE MEASURES	9

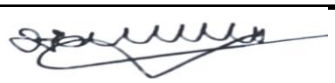
Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors– Multi-vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures.

UNIT-II	PARALLEL PROCESSING, PIPELINING AND ILP	9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors -Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.

UNIT-III	MEMORY HIERARCHY DESIGN	9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cach Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.



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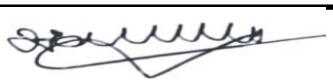
UNIT-IV	MULTIPROCESSORS	9
Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.		

UNIT-V	MULTI-CORE ARCHITECTURES	9
Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture–hp architecture.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Explain the multiprocessors and its performance measure
CO2	Explain the concept of parallel processing and pipelining
CO3	Analyze about the memory hierarchy design
CO4	Outline the issues related to multiprocessors
CO5	Compare multicore architectures
Text Books	
1.	A David E.Culler,JaswinderPalSingh,“Parallel Computing Architecture: A hardware /software approach”, MorganKaufmann / Elsevier,1997
2.	Dimitrios Soudris, Axel Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012.

Reference Books	
1.	Hwang Briggs,“ Computer Architecture and parallel processing”,McGrawHill,1984.
2.	JohnL.Hennessey and David A.Patterson,“ Computer Architecture– A quantitative approach”,MorganKaufmann/Elsevier,4th.Edition,2007.



Approved By BoS Chairman

M.E.	M23AET301-ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURE (Common to AE & VLSI)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To study 80486 and Pentium processor.
2.	To understand CISC and RISC Architectures.
3.	To learn ARM processor.
4.	To learn ARM instruction set.
5.	To study about microcontroller.

UNIT-I	80486 AND PENTIUM PROCESSOR	9

80486 PROCESSOR: Basic programming model – Memory organization – Data types – Instruction set - Addressing mode – Address translation – Interrupts –PENTIUM PROCESSOR Introduction to Pentium processor architecture – Special Pentium Registers– Pentium Memory Management – Introduction to Pentium pro processor – Pentium Pro Special Features.

UNIT-II	CISC AND RISC ARCHITECTURE	9

Introduction to RISC architectures: RISC Versus CISC – RISC Case studies: MIPS R4000 – SPARC – Intel i860 - IBM RS/6000.

UNIT-III	ARM PROCESSOR	9

ARM Programmer's Model – Registers – Processor Modes – State of the processor – Condition Flags – ARM Pipelines – Exception Vector Table – ARM Processor Families – Typical 3 stage pipelined ARM organization–Introduction to ARM Memory Management Unit, Case Study.

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UNIT-IV	ARM ADDRESSING MODES AND INSTRUCTION SET	9
ARM Addressing Modes – ARM Instruction Set Overview – Thumb Instruction Set Overview – LPC210X ARM Processor Features, Case Study.		

UNIT-V	PIC MICROCONTROLLER AND MOTOROLA 68HC11 MICROCONTROLLER	9
Instruction set, addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART. MOTOROLA: CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter – PWM, Case Study.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Outline the basics of 80486 processor
CO2	Explain the functionalities of CISC and RISC architecture
CO3	Analyze the functionalities of ARM processor
CO4	Outline ARM instruction set
CO5	Explain PIC microcontroller and Motorola 68HC11 microcontroller

Text Books	
1.	Andrew Sloss,“ARM System Developers Guide”,Morgan K aufmann Publishers, 2005 approach”,Morgan Kaufmann /Elsevier,1997.
2.	BarryBBrey,“The Intel Microprocessor,Pentium and Pentium ProProcessor,Architecture Programming and Interfacing”, Prentice Hall of India,2002.

Reference Books	
1.	Daniel T abak,“Advanced Microprocessors”, McGraw Hill Inc., 1995.
2.	David E Simon “An Embedded Software Primer ”, Pearson Education,2007.

Approved By BoS Chairman

M.E.	M23AEE103 - NEURAL NETWORKS ANDAPPLICATIONS (Common to AE & VLSI)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To introduce the artificial neural network concepts.
2.	To study various types of artificial neural network architectures.
3.	To study advanced artificial neural network concepts.

UNIT-I	INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS	9
Neuro-physiology - General Processing Element - ADALINE - LMS learning rule - MADALINE – MR2 training algorithm.		

UNIT-II	BPN AND BAM	9
Back Propagation Network - updating of output and hidden layer weights -application of BPN — associative memory - Bi-directional Associative Memory - Hopfield memory -traveling sales man problem		

UNIT-III	SIMULATED ANNEALING AND CPN	9
Annealing, Boltzmann machine - learning - application - Counter Propagation network - architecture -training - Applications.		

UNIT-IV	SOM AND ART	9
Self organizing map - learning algorithm - feature map classifier - applications - architecture of Adaptive Resonance Theory - pattern matching in ART network.		

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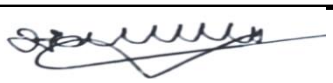
UNIT-V	NEOCOGNITRON	9
Architecture of Neocognitron - Data processing and performance of architecture of spacio – temporal networks for speech recognition.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Explain the concepts of neural networks and different training / learning algorithms
CO2	Design BPNN to solve real time problems
CO3	Apply the concept of counter propagation network for various applications
CO4	Illustrate problem-solving based on pattern matching with specified Self Organizing Map algorithm
CO5	Apply spatial-temporal networks for speech recognition

Text Books	
1.	J.A.Freeman and B.M.Skapura,"Neural Networks, Algorithms Applications and Programming Techniques", Addison-Wesely, 2003.
2.	LaureneFausett,"Fundamentals of Neural Networks: Architecture, Algorithms andApplications",Prentice Hall, 2004

Reference Books	
1.	Simon Haykin, “Neural Networks & Learning Machines”, third edition Pearson Education 2011.
2.	MartinT.Hagan,Howard B.Demuth,MarkBeale,“Neural Network Design”,Thomson 2008.



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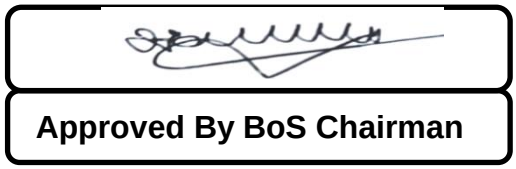
PROFESSIONAL ELECTIVE - II



Approved By BoS Chairman

M.E.	M23VDE202-DSP INTEGRATED CIRCUITS	L	T	P	C
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Course Objectives	
1.	To familiarize the concept of DSP and DSP algorithms.
2.	To introduction to Multirate systems and finite word length effects.
3.	To know about the basic DSP processor architectures.
4.	To study the synthesis of DSP architectures.
5.	To learn the processing elements of DSP architectures.

UNIT-I	INTRODUCTION TO DSP INTEGRATED CIRCUITS	9

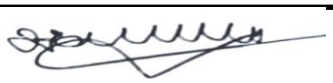
Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT-II	DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS	9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT-III	DSP ARCHITECTURES	9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures



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UNIT-IV	SYNTHESIS OF DSP ARCHITECTURES	9
Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements – clocking of synchronous systems, Asynchronous systems – FSM.		

UNIT-V	ARITHMETIC UNIT AND PROCESSING ELEMENTS	9
Conventional number system, Redundant Number system, Residue Number System, Bit- parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Outline the Digital Signal Processing concepts and its algorithms
CO2	Explain the concept of digital filters
CO3	Compare various DSP architectures
CO4	Analyse the DSP processor architectures and synthesis
CO5	Explain the processing elements and arithmetic unit

Text Books	
1.	B.Venkatramani,M.Bhaskar,“DigitalSignalProcessors”,TataMcGraw-Hill,2002.
2.	JohnJ.Proakis,DimitrisG.Manolakis,“DigitalSignalProcessing”,Pearson Education,2002.

Reference Books	
1.	KeshabParhi, “VLSI Digital Signal Processing Systems design & Implementation”, John Wiley & Sons, 1999.
2.	Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York, 1999.

Approved By BoS Chairman

M.E.	M23VDE203 - NANO ELECTRONICS (Common to VLSI & AE)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To understand the semiconductor nano devices.
2.	To study the materials involved in nano devices.
3.	To learn the operation of nano thermal sensors.
4.	To understand various materials used in gas sensors.
5.	To study the operation of biosensor.

UNIT-I	SEMICONDUCTOR NANO DEVICES	9

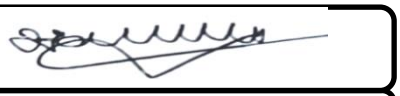
Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nano robotics and Nano manipulation; Mechanical Molecular Nano devices; Nano computers: Optical Fibers for Nano devices; Photochemical Molecular Devices; DNA-Based Nano devices; Gas-Based Nano devices.

UNIT-II	ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS	9

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT-III	THERMAL SENSORS	9

Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.



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UNIT- IV	GAS SENSOR MATERIALS	9
Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity, Discussion of sensors for various gases, Gas sensors based on semiconductor devices.		

UNIT- V	BIO SENSORS	9
Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Classify the types of Nano devices
CO2	Analyze the materials used in Nano device
CO3	Explain the operation of thermal sensor
CO4	Examine the operation of gas sensor
CO5	Outline the operation of bio sensor

Reference Books	
1.	K.E. Drexler, “Nano systems”, Wiley, 1992.
2.	M.C. Petty, “Introduction to Molecular Electronics”, 1995.
3.	W. Ranier, “Nano Electronics and Information Technology”, Wiley, 2003.

Approved By BoS Chairman

M.E.	M23AEE201- HIGH PERFORMANCE NETWORKS (Common to AE & VLSI)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To introduce various systems related to networks.
2.	To study the applications of multimedia networks.
3.	To learn the concept of advanced networks.
4.	To study the various traffic modeling.
5.	To learn about network security in many layers and network management.

UNIT-I	INTRODUCTION	9
Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN, ATM.		

UNIT-II	MULTIMEDIA NETWORKING APPLICATIONS	9
Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.		

UNIT-III	ADVANCED NETWORKS CONCEPTS	9
VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks- P2P connections.		

UNIT-IV	TRAFFIC MODELLING	9
Little's theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.		

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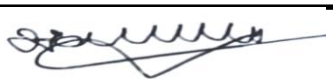
UNIT-V	NETWORK SECURITY AND MANAGEMENT	9
Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Outline the basic high performance network systems
CO2	Explain the applications of multimedia networks
CO3	Analyse the concepts of advanced networks
CO4	Outline the traffic modelling
CO5	Analyse the network security methods

Text Books	
1.	AunuragKumar,D.MAnjunath,JoyKuri,“Communication Networking”,Morgan Kaufmann Publishers,1st Edition, 2004.
2.	Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet”, fifth edition,Pearson Education, 2006.

Reference Books	
1.	HersentGurle& Petit,“IPTelephony,packet Pored Multimedia communication Systems”, Pearson Education, 2003.
2.	J.F.Kurose&K.W.Ross,“Computer Networking - A topdown approach featuring the internet” Pearson,2nd Edition,2003.



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M.E.	M23AEE202 - WIRELESS ADHOC AND SENSOR NETWORKS (Common to AE &VLSI)	L	T	P	C
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Course Objectives	
1.	To understand the basics ofAd-hoc, Sensor Networks and various fundamental and emerging protocols of all layers.
2.	To study about the routing architecture of sensor networks.
3.	To understand the nature and applications of Ad-hoc and sensor networks.
4.	To understand various security practices and protocols of Ad-hoc and Sensor networks.
5.	To understand the basics of Ad-hoc,Sensor Networks and various fundamental and emerging protocols of all layers.

UNIT-I	MAC & TCP IN AD HOC NETWORKS	9

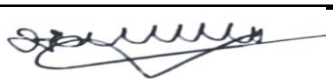
Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.

UNIT-II	ROUTING IN AD HOC NETWORKS	9

Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.

UNIT-III	MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS	9

Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support



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UNIT-IV	SENSOR MANAGEMENT	9
Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators.		

UNIT-V	SECURITY IN ADHOC AND SENSOR NETWORKS	9
Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defense against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Explain the protocols developed for adhoc and sensor networks.
CO2	Analyse different routing approaches
CO3	Outline different architecture in ad hoc and sensor networks.
CO4	Build a Sensor network environment for different type of applications
CO5	Analyse about the security in sensor networks

Text Books	
1.	AdrianPerrig,J.D.Tygar, "Secure Broadcast Communication:In Wired and WirelessNetworks",Springer,2006.
2.	Carlos De MoraisCordeiro,Dharma PrakashAgrawal, “Ad Hoc and Sensor Networks:Theory and Applications (2nd Edition),World Scientific Publishing,2011.

Reference Books	
1.	C.SivaRam Murthy and B.S.Manoj,“AdHoc Wireless Networks-Architectures and Protocols”,Pearson Education,2004.
2.	C.K.Toh,“AdHoc Mobile Wireless Networks”, PearsonEducation,2002.

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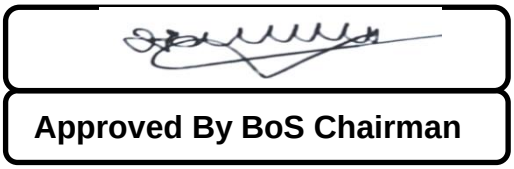
PROFESSIONAL ELECTIVE - III



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M.E.	M23VDE204-SYSTEM ON CHIP DESIGN (Common to VLSI & AE)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To introduce SoC concepts.
2.	To study the system level modelling.
3.	To learn the hardware/software co-design principles.
4.	To familiar with system synthesis.
5.	To learn the hardware/software co-verification principles.

UNIT-I	INTRODUCTION	9

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design.

UNIT-II	SYSTEM LEVEL MODELLING	9

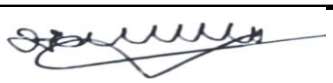
System C: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples.

UNIT-III	HARDWARE SOFTWARE CO-DESIGN	9

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT-IV	SYNTHESIS	9

System synthesis: Transaction Level Modelling (TLM) based design, automaticTLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling.



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UNIT-V	SOC VERIFICATION AND TESTING	9
SoC and IP integration, Verification: Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modelling, test power dissipation, test access mechanism, Case Study.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Outline the basics of SoC design
CO2	Explain the modelling process
CO3	Analyse and design the software hardware models
CO4	Explain the synthesis process
CO5	:Design the test mechanism for SoC test and verification

Text Books	
1.	D.Black,J.Donovan, “System C:From the Ground Up”, Springer,2004.
2.	D.Gajski,S.Abdi,A.Gerstlauer,G.Schirner, “Embedded System Design: Modeling, Synthesis, Verification”, Springer,2009.

Reference Books	
1.	C.SivaRam Murthy and B.S.Manoj,“AdHoc Wireless Networks–Architectures and Protocols”, Pearson Education,2004.
2.	ErikLarson, “Introduction to advanced system-on-chip test design and optimization”,Springer,2005.

Approved By BoS Chairman

M.E.	M23AET201-SOFT COMPUTING AND OPTIMIZATION TECHNIQUES (Common to AE & VLSI)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To understand various neural networks and learning methods.
2.	To overview of Fuzzy logic.
3.	To study the concept of Neuro–Fuzzy modeling.
4.	To introduce the optimization techniques.

UNIT-I	NEURAL NETWORKS	9
Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network.		

UNIT-II	FUZZY LOGIC	9
Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making.		

UNIT-III	NEURO-FUZZY MODELING	9
Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – Case Studies.		

UNIT-IV	CONVENTIONAL OPTIMIZATION TECHNIQUES	9
Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.		

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UNIT-V	EVOLUTIONARY OPTIMIZATION TECHNIQUES	9
Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.		
Total Instructional hours:45		

Course Outcomes: Students will be able to	
CO1	Outline the basics of neural network and learning methods
CO2	Outline the basics of fuzzy logic
CO3	Examine machine learning through Neural Fuzzy concept
CO4	Explain the conventional optimization techniques
CO5	Explain the evolutionary optimization techniques

Text Books	
1.	DavidE.Goldberg,“Genetic Algorithms in Search,Optimization and Machine learning”, Addison wesley, 2009.
2.	George J.Klir and BoYuan,“FuzzySets and FuzzyLogic-Theory and Applications”, PrenticeHall, 1995.

Reference Books	
1.	James A.Freeman and David M.Skapura,“NeuralNetworks Algorithms, Applications,and Programming Techniques”,Pearson Edn.,2003.
2.	Jyh-ShingRogerJang, Chuen-TsaiSun,EijiMizutani,“Neuro-Fuzzy and Soft Computing”, Prentice- Hall of India,2003.

Approved By BoS Chairman

M.E.	M23VDE205 – RECONFIGURABLE ARCH ITECTURES	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To introduce processors and architectures.
2.	To learn about programmed FPGAs.
3.	To study various routing in FPGAs.
4.	To introduce design styles for FPGA.
5.	To familiar with SoPC designs.

UNIT-I	INTRODUCTION	9
Domain-specific processors, Application specific processors, Reconfigurable Computing Systems – Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts & Design steps –classification of reconfigurable architecture-fine, coarse grain & hybrid architectures – Examples.		

UNIT-II	FPGA TECHNOLOGIES & ARCHITECTURE	9
Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.		

UNIT-III	ROUTING FOR FPGAS	9
General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions- Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability- Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks		

Approved By BoS Chairman

UNIT-IV	HIGH LEVEL DESIGN	9
FPGA Design style: Technology independent optimization- technology mapping- Placement. High-level synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.		

UNIT-V	APPLICATION DEVELOPMENT WITH FPGAS	9
Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Illustrate the concepts of reconfigurable architectures
CO2	Explain the FPGA technologies
CO3	Analyze the various routing technologies
CO4	Explain the design styles of FPGA
CO5	Apply the FPGA techniques in solving the real world problems

Text Books	
1.	Christophe Bobda, "Introduction to Reconfigurable Computing –Architectures, Algorithms and Applications", Springer,2010.
2.	CliveMaxfield, "The Design Warrior'sGuidetoFPGAs:Devices,ToolsandFlows",Newnes,Elsevier,2006.

Reference Books	
1.	Jorgen Staunstrup,WayneWlf,"Hardware/Software Co- Design: Principles and practice",Kluwer Academic Pub, 1997.
2.	Maya B.Gokhale and PaulS.Graham,"Reconfigurable Computing: Accelerating Computation with Field-Programmable GateArrays",Springer,2005.

Approved By BoS Chairman

M.E.	M23VDE206 - SIGNAL INTEGRITY FOR HIGH SPEED NETWORKS	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To study the various propagation requirements of transmission lines.
2.	To learn about the multiconductor transmission lines.
3.	To identify the non ideal effects of transmissionlines.
4.	To familiar about the design of transmission line system.
5.	To study the effect of oscillators in transmission lines.

UNIT-I	SIGNAL PROPAGATION ON TRANSMISSION LINES	9

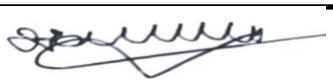
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT-II	MULTI-CONDUCTOR TRANSMISSION LINES AND CROSSTALK	9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT-III	NON-IDEAL EFFECTS	9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tano , routing parasitic, Common-mode current, differential-mode current , Connectors



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UNIT-IV	POWER CONSIDERATIONS AND SYSTEM DESIGN	9
SSN/SSO , DC power bus design , layer stack up, SMT decoupling , Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.		

UNIT-V	CLOCK DISTRIBUTION AND CLOCK OSCILLATORS	9
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Make use of the wave propagation concepts
CO2	Explain about various parameters involved in wave propagation
CO3	Identify the various effects in wave propagation
CO4	Analyse the power issues, jitter and filtering in wave propagation
CO5	Analyse the clocking system for signal transmission

Text Books	
1.	DouglasBrooks,Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR,2003.
2.	EricBogatin,Signal Integrity–Simplified,PrenticeHallPTR,2003.

Reference Books	
1.	H.W.Johnson and M.Graham, High-Speed Digital Design:A Hand book of BlackMagic, Prentice Hall,1993.
2.	S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and DesignPractices,Wiley-Interscience,2000.

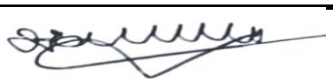
Approved By BoS Chairman

M.E	M23VDP201-VLSI DESIGN LABORATORY - II	L	T	P	C
		0	0	4	2

Course Objectives	
1.	The focus of this course the CAD based VLSI design flow. The entire VLSI design industry makes use of this design flow in some form or the other. Proficiency and familiarity with the various stages of a typical state of this design flow is a prerequisite for any student who wishes to be a part of either the industry or the research in VLSI over one full semester exposure to various stages of a typical state of the art CAD VLSI tool be provided by various experiments designed to bring out the key aspects of simulation, and power and clock routing modules. ASIC RTL realization of an available open source MCU.

List of Experiments	
Expt.No.	**Description of the Experiments (Any 8 experiments)**
1.	To synthesize and understand the Boolean optimization in synthesis.
2.	Static timing analyses procedures and constraints.
3.	Critical path considerations.
4.	Scan chain insertion,Floor planning, Routing and Placement procedures.
5.	Power planning,Layout generation, LVS,back annotation and Total power estimate.
6.	Analog circuit simulation.
7.	Simulation of logic gates, Current mirrors, Current sources and Differential amplifier in Spice.
8.	Layout generations, LVS and Back annotation
	Total Instructional hours:60

Course Outcomes: Students will be able to	
CO1	Apply Boolean optimization concept
CO2	Analyze the timing constraints and procedures
CO3	Examine various floor planning, routing and placement procedures
C04	Test the analog circuits.
C05	Explain about layout generations



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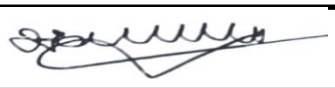
LIST OF EQUIPMENT FOR A BATCH OF 30 STUDENTS		
Sl.No.	**Description of the Equipment**	**Quantity required(Nos.)**
1.	CADENCE / TANNER / Mentor Graphics /Synopses/SPICE Software	15



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M.E.	M23CEP203-ARTICLE WRITING AND SEMINAR (Common to VLSI & AE)	L	T	P	C
		0	0	2	1

Course Objectives	
1.	In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography(atleast15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the author's contributions and critically analyzing each paper.
6. Preparing a working outline
7. Linking the paper sand preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

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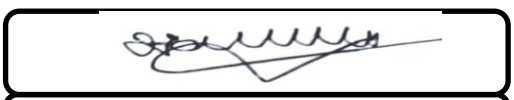
Activity	Instructions	Submission Week	Evaluation Week
Selection of area of interest and Topic (Stating an Objective)	You are requested to select an area of interest, topic and state an objective	2nd week	**3%** Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for 5. Papers (CFP) from your area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)



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Collection of Journal papers in the topic in the context of the objective — collect 20 & then filter	You have to provide a complete list of references you will be using- Based on your objective - Search various digital libraries and Google Scholar When picking papers To read-try to: Pick papers that are Related to each other in Some ways and/or that Are in the same field so That you can write a Meaningful survey out of them, Favour papers from well-known journals and conferences, Favour “first” or “foundational” papers in the field (as indicated in other people"s survey paper),Favour more recent papers, Pick a recent survey of the field so you can quickly Gain an overview, Find relationships with respect to each other and to your topic area (classification Scheme / categorization) Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered	4th week	**6%**(the list of standard papers and reason for selection)

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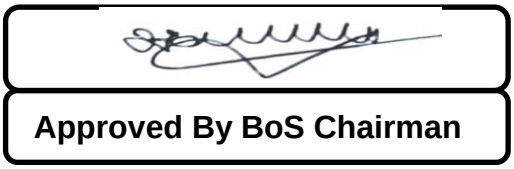
Reading and notes	Reading Paper Process For each paper form a Table answering the following questions: What is the main topic of the article? What was /were the main issue(s) the author said they want to discuss? Why did the author claim it was important? How does the work build on other's work, in the author's opinion? What simplifying assumptions does the author claim to be making? What did the author do? How did the author claim they were going t o evaluate their work and compare it to	5th week	**8%**(the table given should indicate your understanding of the paper and the evaluation is based on your Conclusions about each paper)



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for first 5 papers	others? What did the author say were the limitations of their research? What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper(from the perspective of your survey)		
Reading and notes for next 5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5papers	Repeat Reading Paper Process	7th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification /categorization diagram	8th week	**8%**(this component will be evaluated based on the linking and Classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation &Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%(clarity)**
Sections of the paper	Write the sections of your paper based on the classification/categorization diagram in keeping with the Goal so of your survey	11th week	**10%**(this Component will be evaluated based on the linking and classification Among the papers)
Your conclusions	Write your conclusions and future work	12th week	**5%**(conclusions–clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%**(formatting, English, Clarity and linking) **4%** Plagiarism Check

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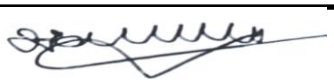
			Report
Seminar	A brief 15 slides on your paper	14th& 15th week	**10%** (based on presentation and Viva-voce)

Course Outcomes: Students will be able to	
CO1	Survey the relevant information
CO2	Outline the importance's
CO3	Formulate the concept
CO4	Compare the data's with existing
CO5	Outline about concluding remarks



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Semester III										
Course Code	**Course Name**	**CT**	**Instructional Hours**					**Assessment**		
			CP	**L**	**T**	**P**	**C**	**CIA**	**ESE**	**Total**
Theory / Theory with Practical										
M23VDT301	Testing of VLSI Circuits	PC	3	3	0	3	3	40	60	100
	Professional Elective -IV	PE	3	3	0	3	3	40	60	100
	Professional Elective-V	PE	3	3	0	3	3	40	60	100
Practical										
M23VDP301	Project Work (Phase I)	PW	12	0	0	12	6	40	60	100
Total credits to be earned							**15**			

Semester IV										
Course Code	**Course Name**	**CT**	**Instructional Hours**					**Assessment**		
			CP	**L**	**T**	**P**	**C**	**CIA**	**ESE**	**Total**
Practical										
M23VDP401	Project Work (Phase II)	PW	24	0	0	24	12	40	60	100
Total credits to be earned							**12**			

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SEMESTER – III										
ELECTIVE – IV										
Course Code	**Course Name**	**CT**	**Instructional Hours**					**Assessment**		
			CP	**L**	**T**	**P**	**C**	**CIA**	**ESE**	**Total**
M23VDE301	Principles of Remote Sensing	PE	3	3	0	0	3	40	60	100
M23AEE303	Advanced Digital Image Processing	PE	3	3	0	0	3	40	60	100
M23AEE304	Pattern Recognition	PE	3	3	0	0	3	40	60	100
M23AET202	Embedded System Design	PE	3	3	0	0	3	40	60	100

SEMESTER – III										
ELECTIVE – V										
Course Code	**Course Name**	**CT**	**Instructional Hours**					**Assessment**		
			CP	**L**	**T**	**P**	**C**	**CIA**	**ESE**	**Total**
M23VDE305	MEMS and NEMS	PE	3	3	0	0	3	40	60	100
M23AET203	Hardware-Software Co-Design	PE	3	3	0	0	3	40	60	100
M23AEE205	Robotics	PE	3	3	0	0	3	40	60	100
M23VDE306	Machine Learning and Algorithm design	PE	3	3	0	0	3	40	60	100

Approved By Chairman

Semester III

Approved By Chairman

B.E	M23VDT301 - TESTING OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

Course Objectives

1.	To understand logic fault models.
2.	To learn test generation for sequential and combinational logic circuits.
3.	To introduce testing designs.
4.	To learn testing algorithms.
5.	To study about the fault diagnosis.

UNIT- I	TESTING AND FAULT MODELLING	9

Introduction to testing – Principle of testing, Types of testing - Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models - Single stuck-at faults.

UNIT- II	TEST GENERATION	9

Algorithms and Representations Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits - Simulation for design verification, test evaluation.

UNIT- III	DESIGN FOR TESTABILITY	9

Design for Testability – Ad-Hoc DFT Methods -Scan Design– generic scan-based design – classical scan-based design– system level DFT approaches.

UNIT- IV	SELF – TEST AND TEST ALGORITHMS	9

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Memory BIST – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT- V	FAULTDIAGNOSIS	9

Diagnostic Test - Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

Total Instructional hours: 45

Approved By Chairman

Reference Books	
1.	A.L.Crouch, “Design Test for Digital ICs and Embedded Core Systems”, Prentice Hall International, 2002.
2.	M. Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
3.	M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed - Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4.	P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

Course Outcomes: Students will be able to	
CO1	Outline the testing and fault modelling.
CO2	Explain the test generation for combinational and sequential circuits.
CO3	Analyse the various testing designs.
CO4	Outline the use of the testing algorithm.
CO5	Explain fault diagnosis.

Approved By Chairman

M.E.	M23VDE301 - PRINCIPLES OF REMOTE SENSING	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To learn physics of remote sensing.
2.	To learn data acquisition.
3.	To study about microwave remote sensing.
4.	To study the principles of thermal sensing.
5.	To learn different technique in data analysis.

UNIT – I	PHYSICS OF REMOTE SENSING	9
Introduction of Remote Sensing - Electro Magnetic Spectrum, Physics of Remote Sensing - Effects of Atmosphere - Scattering – Different types – Absorption - Atmospheric window - Energy interaction with surface features – Spectral reflectance of vegetation, soil and water – atmospheric influence on spectral response patterns - multi concept in Remote sensing.		

UNIT – II	DATA ACQUISITION	9
Types of Platforms – different types of aircrafts - Manned and Unmanned space crafts – sun synchronous and geo synchronous satellites – Types and characteristics of different platforms – LANDSAT, SPOT, IRS, INSAT, IKONOS, QUICKBIRD etc - Opto mechanical and electro optical sensors – multi spectral scanners and thermal scanners – geometric characteristics of scanner imagery - calibration of thermal scanners.		

UNIT – III	SCATTERING SYSTEM	9
Microwave scatterometry – types of RADAR – SLAR – resolution - range and azimuth – real aperture and synthetic aperture RADAR. Characteristics of Microwave images - topographic effect - different types of Remote Sensing platforms – airborne and space borne sensors – ERS, JERS, RADARSAT, RISAT - Scatterometer, Altimeter- LiDAR remote sensing, principles, applications.		

Approved By Chairman

UNIT – IV	THERMAL SENSING	9
Sensors characteristics - principle of spectroscopy - imaging spectroscopy - field conditions, compound spectral curve, Spectral library, radiative models, processing procedures, derivative spectrometry, thermal remote sensing – thermal sensors, principles, thermal data processing, applications.		

UNIT – V	DATA ANALYSIS	9
Resolution – Spatial, Spectral, Radiometric and temporal resolution - signal to noise ratio - visual and digital interpretation – Basic principles of data processing - Radiometric correction - Image enhancement - Image classification – Image Processing software– data merging and biophysical modeling.		
Total Instructional hours: 45		

Course Outcomes : Students will be able to	
CO1	Explain the basic concepts behind remote sensing.
CO2	Examine the data acquisition process of remote sensing.
CO3	Explain the concepts of microwave remote sensing.
CO4	Analyse the sensors used in thermal sensing and its principles.
CO5	Outline remote sensing data analysis methods.

Reference Books	
1.	Lillesand T.M, and Kiefer, R.W, "Remote Sensing and Image interpretation", VI Edition of JohnWiley & Sons, 2000.
2.	John R. Jensen, "Introductory Digital Image Processing: A Remote Sensing Perspective", 2nd Edition, 1995.
3.	John A.Richards, "Remote Sensing Digital Image Analysis", Springer –Verlag,1999
4.	Paul Curran P.J, "Principles of Remote Sensing", ELBS, 1995.
5.	Charles Elachi and Jakob J. van Zyl, "Introduction To The Physics and Techniques of Remote Sensing", Wiley Series in Remote Sensing and Image Processing, 2006.
6.	Sabins, F.F.Jr, "Remote Sensing Principles and Image interpretation", W.H.Freeman & Co, 1978.

Approved By Chairman

B.E	M23AEE303 – ADVANCED DIGITAL IMAGE PROCESSING	L	T	P	C
		3	0	0	3

Course Objectives

1.	To understand the fundamentals of digital image processing.
2.	To learn concept of color image processing technique.
3.	To learn morphological image processing algorithms.
4.	To learn segmentation algorithms and descriptors for image processing.
5.	To study object recognition and image processing applications.

UNIT- I	FUNDAMENTALS OF DIGITAL IMAGE PROCESSING	9

Elements of Visual Perception- Image acquisition, digitization- Histogram - Image enhancement – Spatial filters for smoothing and sharpening – Discrete 2D transforms - DFT, DCT, Walsh-Hadamard, Slant, KL, Wavelet Transform – Haar wavelet.

UNIT- II	COLOR IMAGE PROCESSSING	9

Color Image Fundamentals-Color Models- RGB, CMY, CMYK and HSI Color Models- Pseudocolor Image Processing - Intensity Slicing- Intensity to Color transformations -Basics of Color Image Processing- Color Transformation - Color Image Smoothing and Sharpening- Color Segmentation - Noise in Color Images.

UNIT- III	MORPHOLOGICAL IMAGE PROCESSING	9

Preliminaries- Basic Concepts from Set Theory-Logic Operations Involving Binary Images - Dilation and Erosion –Opening and Closing - Hit-or-Miss Transformation - Basic Morphological Algorithms - Boundary Extraction- Region Filling- Extraction of Connected Components- Convex Hull- Thinning- Thickening- Skeletons- Pruning- - Gray-Scale Morphology, Case Study

UNIT- IV	SEGMENTATION, REPRESENTATION AND DESCRIPTION	9

Edge Detection - Edge Linking and Boundary Detection -Thresholding- Segmentation by Morphological Watershed Segmentation Algorithm - Use of Markers- Representation and Boundary Descriptors, Case Study.

UNIT- V	3D IMAGE VISUALIZATION	9

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, multiply connected surfaces, Image processing in 3D, Measurements on 3D images.

Total Instructional hours: 45

Approved By Chairman

Reference Books	
1.	Rafael C. Gonzalez, "Digital Image Processing", Pearson Education, Inc., 3rd Edition, 2008.
2.	Milman Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis and Machine Vision", Brooks/Cloe, Vikas Publishing House 2nd Edition, 1999.
3.	Khalid Sayood, "Data Compression", Morgan Kaufmann Publishers (Elsevier)., 3rd Edition, 2006.
4.	Rafael C. Gonzalez, Richards E.Woods, Steven Eddins, "Digital Image Processing using MATLAB", Pearson Education, Inc., 2004.
5.	Willam K.Pratt, "Digital Image Processing", John Wiley, New York, 2002.
6.	Rick S.Blum, Zheng Liu," Multisensor image fusion and its Applications", Taylor & Francis, 2006.

Course Outcomes: Students will be able to	
CO1	Explain about image acquisition, digitization and spatial filters for enhancement
CO2	Outline color image processing techniques
CO3	Apply morphological image processing algorithms
CO4	Apply segmentation algorithms and descriptors for image processing
CO5	Examine neural networks, fuzzy logic, genetic algorithms in object recognition,compression, watermarking and steganography algorithms to images

Approved By Chairman

B.E	M23AEE304 - PATTERN RECOGNITION	L	T	P	C
		3	0	0	3

Course Objectives

1.	To learn about supervised pattern classifiers.
2.	To learn about unsupervised pattern classifiers.
3.	To familiarize about different feature extraction techniques.
4.	To explore the role of Hidden Marko model and SVM in pattern recognition.
5.	To study the application of Fuzzy logic and Neural Network for pattern classifier.

UNIT- I	PATTERN CLASSIFIER	9

Overview of Pattern recognition – Discriminant functions – Supervised learning –Parametric estimation – Maximum Likelihood Estimation – Bayes Theorem – Bayesian Belief Network, Naive Bayesian Classifier.

UNIT- II	CLUSTERING	9

Clustering for unsupervised learning and classification–Clustering concept-Types of Clustering – C Means algorithm –Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT- III	FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION	9

Principle component analysis, Independent component analysis, Linear discriminant analysis, Feature selection through functional approximation – Elements of formal grammars, Syntactic description – Stochastic grammars – Structural Representation, Case Study.

UNIT- IV	HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE	9

State Machines – Hidden Markov Models – Training – Classification – Support vector Machine – Feature Selection, SVM Applications.

UNIT- V	RECENT ADVANCES	9

Fuzzy Set Theory, Fuzzy and Crisp Classification, Fuzzy Clustering, – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception-Elementary Neural Network for Pattern Recognition-ADALINE.

Total Instructional hours: 45

Approved By Chairman

Reference Books	
1.	Andrew Webb, “Stastical Pattern Recognition”, Arnold publishers, London, 1999.
2.	C.M. Bishop, “Pattern Recognition and Machine Learning”, Springer, 2006.
3.	M. Narasimha Murthy and V. Susheela Devi, “Pattern Recognition”, Springer, 2011.
4.	Menahem Friedman and Abraham Kandel, “Introduction to Pattern Recognition Statistical, Structural, Neural and Fuzzy Logic Approaches”, World Scientific publishing Co. Ltd, 2000.
5.	Robert J.Schalkoff, “Pattern Recognition Statistical, Structural and Neural Approaches”, John Wiley & Sons Inc., New York, 1992.
5.	R.O. Duda, P.E.Hart and D.G.Stork, “Pattern Classification”, John Wiley, 2001.
7.	S.Theodoridis and K.Koutroumbas, “Pattern Recognition”, 4th Ed., Academic Press, 2009.

Course Outcomes: Students will be able to	
CO1	Outline the concepts of supervised classifiers.
CO2	Outline the concepts of Clustering.
CO3	Classify the data and identify the patterns.
CO4	Make use of feature set and select the features from given data set.
CO5	Apply fuzzy logic and genetic algorithms for classification problems.

M.E.	M23AET202-EMBEDDED SYSTEM DESIGN (Common to AE and VLSI)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To introduce the overview, design metrics and methodology of embedded systems.
2.	To introduce architecture of single purpose processor.
3.	To understand various protocols of embedded system.
4.	To understand the State machine models.
5.	To introduce software development tools

UNIT- I	EMBEDDED SYSTEM OVERVIEW	9

Embedded System Overview, Design Challenges — Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT-II	GENERAL AND SINGLE PURPOSE PROCESSOR	9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application – Specific Instruction- Set Processors(ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT-III	BUS STRUCTURES	9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus- Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARMBus, Wireless Protocols–IrDA,Bluetooth,IEEE802.11.

UNIT-IV	STATE MACHINE AND CONCURRENT PROCESSMODELS	9

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-:Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT-V	EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	9
Compilation Process – Libraries – Porting kernels – C extensions for embedded systems –emulation and debugging techniques–RTOS–System design using RTOS.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Explain the design challenges and basic metrics of embedded system
CO2	Explain the architecture and pipelining process
CO3	Analyse different protocols
CO4	Examine the state machine and design process models.
CO5	Outline embedded software development tools and RTOS.

Reference Books	
1.	Bruce Powel Douglas,"Realtime UML,second edition: Developing efficient objects for embedded systems",3rdEdition 1999, Pearson Education.
2.	Daniel W.Lewis," Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.
3.	Frank Vahidand Tony Gwargie,"Embedded System Design", John Wiley &sons,2002.
4	SteveHeath,"Embedded System Design", Elsevier, Second Edition,2004.
5	Bruce Powel Douglas,"Realtime UML,second edition: Developing efficient objects for embedded systems",3rdEdition1999,Pearson Education.

B.E	M23VDE305 - MEMS AND NEMS	L	T	P	C
		3	0	0	3

Course Objectives

1.	To introduce the concepts of micro-electromechanical devices.
2.	To know the fabrication process of Microsystems.
3.	To know the design concepts of micro sensors.
4.	To know the design concepts of micro actuators.
5.	To familiarize concepts of quantum mechanics and nano systems.

UNIT- I	INTRODUCTION AND FABRICATION OF MEMS	9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro-accelerometers and Micro fluidics, Materials for MEMS: Silicon, silicon compounds, polymers, metals. Photolithography, Ion Implantation, Diffusion, Oxidation, Dry and wet etching, Bulk Micromachining, Surface Micromachining, LIGA.

UNIT- II	INTRODUCTION AND FABRICATION OF NEMS	9

Introduction to NEMS, Nano scaling, classification of nano structured materials, Applications of nanomaterials. Synthesis routes – Bottom up and Top down approaches. Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation.

UNIT- III	DESIGN OF MEMS SENSORS AND ACTUATORS	9

Acoustic sensor – Quartz crystal microbalance, Surface acoustic wave, Flexural plate wave, shear horizontal; Vibratory gyroscope, Pressure sensors, Electrostatic actuators, piezoelectric actuators, Thermal actuators, Actuators using shape memory alloys, Microgrippers, Micromotors, Microvalves, Micropumps.

UNIT- IV	RF AND BIO MEMS	9

Introduction to RF MEMS technologies: Need for RF MEMS components in communications, space and defense applications, Materials and fabrication technologies, Special considerations in RF MEMS design. Case studies: Micro-switches BioMEMS- Drug delivery, Electronic nose, Bio chip.

UNIT- V	NANOSYSTEMS AND QUANTUM MECHANICS	9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

Total Instructional hours: 45

Reference Books	
1.	Ran Hsu, MEMS and Microsystems Design and Manufacture, Tata McGraw Hill, 2002.
2.	Murty B.S, Shankar P, Raj B, Rath, B.B, Murday J, Textbook of Nanoscience and Nanotechnology, Springer publishing, 2013
3.	Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures",CRC Press, 2002
4.	Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.
5.	Vinod Kumar Khanna Nanosensors: Physical, Chemical, and Biological, CRC press,2012.
6.	Mahalik N P, MEMS, Tata McGraw Hill, 2007.
7.	Manouchehr E Motamedi, MOEMS: Micro-Opto-Electro-Mechanical Systems, SPIE press, First Edition, 2005.

Course Outcomes: Students will be able to	
CO1	Outline the concepts of micro-electromechanical devices
CO2	Explain the fabrication process of Microsystems
CO3	Design the concepts of micro sensors
CO4	Design the concepts of micro actuators
CO5	Explain concepts of quantum mechanics and nano systems

M.E.	M23AET203 – HARDWARE-SOFTWARE CO- DESIGN (Common to VLSI & AE)	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To acquire the knowledge about system specification and modelling.
2.	To learn the formulation of partitioning.
3.	To learn the co-synthesis.
4.	To study the different technical aspects about proto typing and emulation.
5.	To introduce the design specification and verification.

UNIT- I	SYSTEM SPECIFICATION AND MODELLING	9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling,Co-Design for Heterogeneous Implementation-Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification

UNIT- II	HARDWARE / SOFTWARE PARTITIONING	9

The Hardware /Software Partitioning Problem, Hardware –Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms

UNIT- III	HARDWARE/SOFTWARE CO-SYNTHESIS	9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

UNIT- IV	PROTOTYPING AND EMULATION	9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture-Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems.

UNIT- V	DESIGN SPECIFICATION AND VERIFICATION	9
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification ,Design Representatio for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification an Multi-Language Co-simulation.		
		Total Instructional hours:45

Course Outcomes: Students will be able to	
CO1	Outline the system specification and modeling
CO2	Explain the partitioning and scheduling Algorithm
CO3	Explain the co-synthesis algorithm
CO4	Compare various architectures of prototyping and emulation
CO5	Analyze about the design specification and validate its functionality by simulation

Reference Books	
1.	Giovanni De Micheli,Rolf Ernst Morgon,"Reading in Hardware/Software Co-Design",KaufmannPublishers,2001.
2.	Jorgen Staun strup,WayneWolf, "Hardware / Software Co-Design": Principles and Practice",Kluwer Academic Pub,1997.
3.	RalfNiemann,"Hardware / Software Co-Design for Data Flow Dominated Embedded Systems",Kluwer Academic Pub,1998.
4	Giovanni De Micheli, Rolf Ernst Morgon,"Reading in Hardware / Software Co-Design", Kaufmann Publishers,2001.

M.E.	M23AEE205–ROBOTICS	L	T	P	C
		3	0	0	3

Course Objectives	
1.	To understand robot locomotion and mobile robot kinematics.
2.	To understand perception in robotics.
3.	To study mobile robot localization
4.	To learn the mobile robot mapping.
5.	To study robot planning and navigation

UNIT - I	LOCOMOTION AND KINEMATICS	9

Introduction to Robotics–key issues in robot locomotion–legged robots–wheeled mobile robots — aerial mobile robots — introduction to kinematics — kinematics models and constraints–robot maneuverability

UNIT-II	ROBOT PERCEPTION	9

Sensors for mobile robots–vision for robotics–cameras–image formation–structure from stereo–structure from motion–optical flow–color tracking–place recognition–range data.

UNIT-III	MOBILE ROBOT LOCALIZATION	9

Introduction to localization–challenges in localization–localization and navigation–belief representation – map representation – probabilistic map-based localization – Markov localization — EKF localization — UKF localization — Grid localization — Monte Carlolocalization–localization in dynamic environments.

UNIT-IV	MOBILE ROBOT MAPPING	9

Autonomous map building–occupancy grip mapping–MAP occupancy mapping–SLAM,–extended Kalman Filter SLAM — graph-based SLAM — particle filter SLAM— sparse extended information filter–fast SLAM algorithm.

UNIT-V	PLANNING AND NAVIGATION	9
Introduction to planning and navigation–planning and reacting–path planning–obstacle avoidance techniques–navigation architectures–basic exploration algorithms.		
		Total Instructional hours:45

Course Outcomes:Students will be able to	
CO1	Explain robot locomotion, kinematics models and constraints.
CO2	Analyze the vision algorithms for robotics
CO3	Test robot localization techniques
CO4	Test robot mapping techniques
CO5	Analyze the planning and exploration algorithms

Reference Books	
1.	Gregory Dudek and MichaelJenkin,"Computational Principles of Mobile Robotics", Second Edition,Cambridge University Press,2010.
2.	Howie Chosetet al., "Principles of Robot Motion: Theory, Algorithms, and Implementations", ABradford Book, 2005
3.	MajaJ. Mataric,"The Robotics Primer", MIT Press, 2007.
4.	RolandSeigwart, IllahReza Nourbakhsh, and Davide Scaramuzza,"Introduction to autonomous mobile robots",Second Edition, MIT Press,2011.
5.	SebastianThrun,WolframBurgard, and DieterFox,"Probabilistic Robotics", MIT Press, 2005.

B.E	M23VDE306 – MACHINE LEARNING AND ALGORITHM DESIGN	L	T	P	C
		3	0	0	3

Course Objectives

1.	To understand the concepts and mathematical foundations of machine learning and types of problems tackled by machine learning
2.	To explore the different supervised learning techniques including ensemble methods
3.	To learn different aspects of unsupervised learning and reinforcement learning
4.	To compare the k means and hierarchal clustering technique
5.	To know the selection of algorithm for specific applications.

UNIT- I	INTRODUCTION AND MATHEMATICAL FOUNDATIONS	9

What is Machine Learning? Need –History – Definitions – Applications - Advantages, Disadvantages & Challenges -Types of Machine Learning Problems – Mathematical Foundations - Linear Algebra & Analytical Geometry -Probability and Statistics- Bayesian Conditional Probability -Vector Calculus & Optimization - Decision Theory - Information theory

UNIT- II	SUPERVISED LEARNING	9

Introduction-Discriminative and Generative Models -Linear Regression - Least Squares -Under-fitting / Overfitting -Cross-Validation – Lasso Regression- Classification - Logistic Regression- Gradient Linear Models -Support Vector Machines –Kernel Methods -Instance based Methods - K-Nearest Neighbors - Tree based Methods –Decision Trees –ID3 – CART - Ensemble Methods –Random Forest - Evaluation of Classification Algorithms

UNIT- III	UNSUPERVISED LEARNING AND REINFORCEMENT LEARNING	9

Introduction - Clustering Algorithms -K – Means – Hierarchical Clustering - Cluster Validity - Dimensionality Reduction –Principal Component Analysis – Recommendation Systems - EM algorithm. Reinforcement Learning – Elements -Model based Learning – Temporal Difference Learning IC.

UNIT- IV	MAIN ALGORITHMS USED IN ML	9

Linear Regression, Decision Trees, K-nearest Neighbour, Collaborative Filtering, Dimensionality Reduction Technique, Logistic Regression, Support Vector Machine.

UNIT- V	NAIVES BAYES	9

Conditional Probability and Its Intuition, Bayes' Theorem, Naive Bayes -With One Feature, Conditional Independence in Naive Bayes, Deciphering Naive Bayes, Introduction - Naive Bayes for Text Classification, Document Classifier - Pre Processing Steps, Document Classifier - Worked out Example, Laplace Smoothing.

Total Instructional hours: 45

Text Books	
1.	APPLIED MACHINE LEARNING by M. GOPAL, MC GRAW HILL
2.	Marc Peter Deisenroth, A. Aldo Faisal, Cheng Soon Ong, Mathematics for Machine Learning, Cambridge University Press (23 April 2020)
3.	Tom M. Mitchell- Machine Learning - McGraw Hill Education, International Edition

Reference Books	
1.	Introduction To Machine Learning With Python by Andreas C. Müller, SARAH GUIDO, O Reilly Publishing.
2.	Trevor Hastie, Robert Tibshirani, and Jerome Friedman - The Elements of Statistical Learning: Data Mining, Inference, and Prediction - Springer, 2nd edition.

Course Outcomes: Students will be able to	
CO1	Understand the fundamental concepts and mathematical foundations of machine learning and types of problems tackled by ML techniques
CO2	Applying different supervised learning techniques like Regression, Classification and SVM including ensemble methods
CO3	Analyzing different unsupervised learning techniques and reinforcement learning.
CO4	Appreciate the mathematical background behind popular ML algorithms.
CO5	Ensure awareness about importance of conditional algorithms, Classifier and Naive Bayes concepts in ML

M.E.	M23VDP301 - PROJECT WORK (PHASE I)	L	T	P	C
		0	0	12	6

Course Objectives:

1. To enable a student to do an individual project work this may involve design,modelling, simulation and/or fabrication.
2. To analyse a problem both theoretically and practically.
3. To motivate the students to involve in research activities leading to innovativesolutions for industrial and societal problems.

COURSE DESCRIPTION:

Project work shall be carried out by each and every individual student under the supervision of a faculty of this department. A student may however, in certain cases, be permitted to work for the project in association with other departments or in an Industrial/Research Organization, on the recommendation of the Head of the Department. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist from the organization. The student shall meet the supervisor periodically and attend the periodic reviews for evaluating the progress.

Project work will be carried out in two phases, Phase-I during the third semester and Phase-II during the final semester. Phase-I shall be pursued for a minimum of 12 periods per week and Phase — II in 24 periods per week. In each phase, there will be three reviews for continuous internal assessment and one final review and viva voce at the end of the semesters. The Project Report prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department.

Course Outcomes:

Students will be able to

CO1: Identify the area, narrow dine the problem and understand the problem thoroughly and provide an appropriate solution.

CO2: Show the systematic literature survey which helps to build the knowledge in the chosen field by using the existing journal references

CO3: Construct a mathematical model for the system under study.

CO4: Choose and get proficiency over the software for simulation and analysis.

CO5: Utilize the findings of the phase I work in conferences/journals.

Semester-IV

M.E.	M23VDP401 - PROJECT WORK (PHASE II)	L	T	P	C
		0	0	24	12

Course Objectives:

1. To enable a student to do an individual project work this may involve design,modelling, simulation and/or fabrication.
2. To analyse a problem both theoretically and practically.
3. To motivate the students to involve in research activities leading to innovativesolutions for industrial and societal problems.

COURSE DESCRIPTION:

Project work shall be carried out by each and every individual student under the supervision of a faculty of this department. A student may however, in certain cases, be permitted to work for the project in association with other departments or in an Industrial/Research Organization, on the recommendation of the Head of the Department. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist from the organization. The student shall meet the supervisor periodically and attend the periodic reviews for evaluating the progress.

Project work will be carried out in two phases, Phase-I during the third semester and Phase-II during the final semester. Phase-I shall be pursued for a minimum of 12 periods per week and Phase — II in 24 periods per week. In each phase, there will be three reviews for continuous internal assessment and one final review and viva voce at the end of the semesters. The Project Report prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department.

Course Outcomes:

Students will be able to

CO1: Identify the area, narrow dine the problem and understand the problem thoroughly and provide an appropriate solution.

CO2: Show the systematic literature survey which helps to build the knowledge in the chosen field by using the existing journal references

CO3: Construct a mathematical model for the system under study.

CO4: Choose and get proficiency over the software for simulation and analysis.

CO5: Utilize the findings of the phase I work in conferences/journals.